a first strongly doped region of said second conduction type that is introduced into said surface of said semiconductor substrate and is electrically connected to a first terminal;

a second strongly doped region of said first conduction type that is introduced into said well region and is electrically connected to a second terminal;

a third strongly doped region of said second conduction type, which is introduced into said well region, and is electrically connected to said second terminal; and

a fourth strongly doped region of said second conduction type, which is introduced into said surface of said semiconductor substrate and into said well region, and is spatially situated above a pn junction that is formed between said semiconductor substrate and said well region, and between said third strongly doped region and said first strongly doped region.

2.(Previously Amended) The lateral thyristor structure of claim 1, comprising a field oxide region that is situated between said first strongly doped region and said fourth strongly doped region.

3.(Previously Amended) The lateral thyristor structure of claim 1, comprising a field oxide region that is situated between said second strongly doped region and said fourth strongly doped region.

4.(Original) The lateral thyristor structure of claim 3, wherein said first conduction type is p-conducting and said second conduction type is n-conducting.

5.(Original) The lateral thyristor structure of claim 4, wherein said first terminal is connected to ground, and said second terminal is connected to a signal input line or to a signal output line.

6.(Cancelled)

7.(Previously Cancelled)

8.(Currently Amended) The lateral thyristor structure of claim 5~~6~~, wherein said at least two lateral thyristors are surrounded by a substrate contact ring.

9.(Currently Amended) The lateral thyristor structure of claim 5~~6~~, wherein said at least two lateral thryristors are arranged symmetrically.

10.(Cancelled)

11.(Cancelled)

12.(Currently Amended) A symmetrical lateral thyristor structure for protection against electrostatic discharge, comprising:

at least two lateral thyristors, which each include

a semiconductor substrate of a first conduction type, with a surface;

a well region of a second conduction type, opposite to said first conduction type, which is introduced into said surface of said semiconductor substrate;

a first strongly doped region of said second conduction type that is introduced into said surface of said semiconductor substrate and is electrically connected to a first terminal;

a second strongly doped region of said ~~second~~ first conduction type that is introduced into said well region and is electrically connected to a second terminal;

a third strongly doped region of said second conduction type, which is introduced into said well region, and is electrically connected to said second terminal; and

a fourth strongly doped region of said second conduction type, which is introduced into said surface of said semiconductor substrate and into said well region, and is spatially situated above a pn junction that is formed between said semiconductor substrate and said well region, and between said third strongly doped region and said first strongly doped region.